Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A linear scalable method of processing a digital signal under control of instructions executing on a multiprocessor computing system by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) ~~in a multiprocessing system~~ of the digital signal using a decimation in time approach, comprising the steps of:

computing an N-point FFT/IFFT of the signal using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix;

distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage; and

storing the transformed ~~signal.~~ signal in a memory.

2. (Previously Presented) A linear scalable method as claimed in claim 1 wherein said step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

3. (Currently Amended) A linear scalable system to process a digital signal by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the signal in a multiprocessing system using a decimation in time approach, comprising:

means for computing a plurality of stages of an N-point FFT/IFFT of the signal using in each stage of the plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop of a first radix and without employing nested loops;

means for distributing the butterfly operations in each stage of the plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage; and

~~means~~ a memory for storing inputs and output of the means for computing.

4. (Previously Presented) A linear scalable system as claimed in claim 3 wherein said means for distributing the butterfly operations is implemented by means for assigning to each processor of the multi-processor system respective addresses of memory locations in the means for storing inputs and outputs corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

5. (Currently Amended) A computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal by computing with the plurality of processors a Fast Fourier Transform (FFT) or an Inverse Fast Fourier Transform (IFFT) of the signal using a decimation in time approach, the method comprising:~~A computer program product comprising computer readable program code stored on a computer readable storage medium embodied therein for processing a digital signal by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the signal in a multiprocessing system using a decimation in time linear scalable approach, comprising:~~

~~computer readable program code means configured for~~ computing first and second stages of $\log_2 N$ stages of an N-point FFT/IFFT as a single radix-4 butterfly operation

while implementing the remaining ($\log_2$N-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops;

~~computer readable program code means configured for~~ distributing the butterfly operations in each stage such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage; and

~~computer readable program code means configured for~~ storing the transformed ~~signal.~~ signal in a memory.

6. (Currently Amended) The computer computer-readable memory medium of ~~program product as claimed in~~ claim 5 wherein ~~said computer readable program code means configured for~~ distributing the butterfly operations ~~is implemented by computer readable program code means configured for~~comprises assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

7. (Previously Presented) The method of claim 1 wherein the first radix is a radix-2 radix.

8.-9. (Canceled)

10. (Previously Presented) The method of claim 1 wherein an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT.

11. (Previously Presented) The method of claim 2, wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

12. (Previously Presented) The system of claim 3 wherein the first radix is a radix-2 radix.

13. (Previously Presented) The system of claim 12 wherein the plurality of stages comprises $\log_2 N$-2 stages, further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation.

14. (Previously Presented) The system of claim 3 wherein the first plurality of stages comprises $\log_2 N$-2 stages.

15. (Previously Presented) The system of claim 4 wherein the means for assigning is configured to insert a binary digit in an address of a memory location.

16. (Currently Amended) A computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal, the method comprising:

computing an N-point FFT/IFFT using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage of the first plurality of stages has a single, un-nested computation loop of the first radix;

distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage; and

storing the transformed ~~signal.~~ signal in a memory.

17. (Previously Presented) The computer-readable memory medium of claim 16 wherein the distributing butterfly operations in each stage comprises assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

18. (Previously Presented) The computer-readable memory medium of claim 17 wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

19. (Previously Presented) The computer-readable memory medium of claim 16 wherein the first plurality of stages comprises $\log_2 N$-2 stages.

20. (Previously Presented) The computer-readable memory medium of claim 16 wherein an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT.

21-23. (Canceled)

24. (New) The method of claim 1, further comprising configuring the multiprocessor system to perform spectral analysis on the digital signal.

25. (New) The method of claim 1, further comprising configuring the multiprocessor system to filter the digital signal in a frequency domain.

26. (New) The method of claim 1, further comprising configuring the multiprocessor system to perform polyphase transformations.

27. (New) A method of transforming a digital signal, the method comprising:

computing, with a multiprocessor computing system having a plurality of processors P, a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT);

computing remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a

single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop; and

storing the transformed digital signal in a memory medium.

28. (New) The method of claim 27 wherein the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage.

29. (New) The method of claim 27 wherein the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages.

30. (New) The method of claim 27 wherein transforming the digital signal comprises filtering the digital signal in a frequency domain.

31. (New) A system, comprising:

an instruction fetch cache; and

a plurality P processors coupled to the instruction fetch catch and configured to:

compute a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier Transform (IFFT) of a digital signal; and

compute remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop.

32. (New) The system of claim 31 wherein the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage.

33. (New) The system of claim 31 wherein the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages.

34. (New) The system of claim 31 wherein the system is configured to filter a digital signal in a frequency domain.